Customer No.: 31561
Application No.: 10/605,275
Docket No.: 11241-US-PA

Claim Amendment

Please amend the claims in the application according to the following listing of claims.

1. (original) A quad flat no-lead chip carrier, comprising:

a conductive plate having a first surface and a second surface, wherein the first surface has a chip-bonding region and the conductive plate furthermore has a plurality of columnar through holes located on the periphery of the chip-bonding region such that the columnar through holes pass through the conductive plate to link up the first and the second surfaces;

a plurality of conductive columns set up within the respective columnar through holes; and

a plurality of dielectric walls set up between the sidewall of the conductive columns and the inner surface of corresponding columnar through holes.

2. (original) The chip carrier of claim 1, wherein the first surface of the conductive plate is a rough surface.

3. (original) The chip carrier of claim 1, wherein the first surface of the conductive plate has an oxide layer thereon.

4. (original) The chip carrier of claim 1, wherein the carrier further comprises a solder mask layer set up on the second surface of the conductive plate that exposes a portion of an end surface of the conductive columns near the second surface.

5. (currently amended) A quad flat no-lead chip package, comprising:

a chip carrier comprising:

a conductive plate having a first surface and a second surface, wherein the first surface has a chip-bonding region and the conductive plate furthermore has a plurality of columnar through holes located on the periphery of the chip-bonding region such that the columnar through holes pass through the conductive plate to link up the first and the second surface;

a plurality of conductive columns set up within the respective columnar through holes; and

a plurality of dielectric walls set up between the sidewall of the conductive columns and the inner surface of the corresponding columnar through holes;

a chip attached to the chip-bonding region on the first surface of the conductive plate;

a plurality of first conductive wires electrically connecting the chip and the conductive columns; and

an insulating material enclosing the chip and the first conductive wires.

6. (original) The chip package of claim 5, wherein the package further comprises at least a second conductive wire electrically connecting the chip to the conductive plate.

7. (original) The chip package of claim 5, wherein the package further comprises a conductive paste layer sandwiched between the chip and the conductive plate.

8. (original) The chip package of claim 5, wherein the first surface of the conductive plate is a rough surface.

9. (original) The chip package of claim 5, wherein the first surface of the conductive plate has an oxide layer thereon.

10. (original) The chip package of claim 5, wherein the carrier further comprises a solder mask layer set up on the second surface of the conductive plate that exposes a portion of an end surface of the conductive columns near the second surface.

Claim 11 (new) A quad flat no-lead chip carrier, comprising:

a conductive plate having a first surface and a second surface, wherein the first surface has a chip-bonding region and the conductive plate further has a plurality of columnar through holes located on the periphery of the chip-bonding region such that the columnar through holes pass through the conductive plate to link up the first and the second surfaces;

a plurality of solid conductive columns disposed within the respective columnar through holes;

a plurality of dielectric walls disposed between the sidewall of the conductive columns and the inner surface of the corresponding columnar through holes , wherein the dielectric walls are disposed within the corresponding columnar through holes; and

a chip attached to the first surface of the conductive plate through a plurality of conductive wires connecting the chip and the conductive columns.

Claim 12(new) The quad flat no-lead chip carrier of claim 11, wherein the solid conductive columns completely fill the corresponding columnar through holes.

Claim 13 (new) The quad flat no-lead chip carrier of claim 11, wherein the carrier further comprises a solder mask layer configured on the second surface of the conductive plate that exposes a portion of an end surface of the conductive columns near the second surface.

Claims 14 (new) The quad flat no-lead chip carrier of claim 11, wherein the first surface of the conductive plate is a rough surface.

Claim 15 (new) The quad flat no-lead chip carrier of claim 11, wherein the first surface of the conductive plate has an oxide layer thereon.

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Present Status of the Application

This is a full and timely response to the outstanding non-final Office Action mailed on June 30, 2004. The Office Action has rejected claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over Kiumura (US Patent Application 2003/0151139) in view of admitted prior art and further in view of Kikuchi et al. (USP 5122860) and Murata (USP 6400010).

Claims 1-10 remain pending and claims 11-15 are newly added to more accurately describe the invention. It is believed that no new matter is added by way of these amendments made to the claims or otherwise to the application.

Applicant has most respectfully considered the remarks set forth in this Office Action. Regarding the obvious rejections, it is however strongly believed that the cited references are deficient to adequately teach the claimed features as recited in the presently pending claims. The reasons that motivate the above position of the Applicant are discussed in detail hereafter, upon which reconsideration of the claims is most earnestly solicited.

Response to 35 U.S.C. 103 rejection

Claims 1, 3, 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiumura (US Patent Application 2003/0151139) in view of admitted prior art (APA).

To establish a prima facie case of obviousness under 35 U.S.C.§ 103(a), the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Applicants respectfully submit that Kiumura in view of APA is legally deficient for the purpose of rendering claims 1 & 5 unpatentable for the reasons discussed hereinafter.

The present invention, as basically recited in claims 1 & 5, at least teaches 'a plurality of conductive columns set up within the respective columnar through holes; and a plurality of dielectric walls set up between the sidewall of the conductive columns and the inner surface of corresponding columnar through holes'

The Office alleges that the conductive layer 110 on the surface of the solder ball supporting hole 112e and the solder balls 111 mounted on the outside surface of the solder ball supporting hole 112e of Kiumura as being equivalent to the conductive columns of this invention. Applicant respectfully disagrees because conductive columns, by definition, are structure consisting of a cylindrical shaft (Webster dictionary, 3rd edition). The conductive layer 110 of Kiumura is a thin liner type layer, formed only on the surface of the supporting hole 112e, and the solder ball 111 is hemispherical shape (see. Figs. 1 & 7). Therefore, the conductive layer 110 and the solder ball 111 of Kiumura can not constitute as the conductive columns of this invention. Further, the present invention teaches the plurality of conductive columns set up within the respective columnar through holes. Kiumura, on the other hand, fails to explicitly teach or implicitly suggest these claimed

features. First of all, Kiumura does not teach columnar through holes. Kiumura instead teaches, as in paragraph [0036], that these holes are hanging bell shaped holes (112+113). Second, the conductive layer 110 of Kiumura is also formed on the lower surface of the substrate 109, outside the hanging bell shaped holes (112 + 113) (see Figs. 5-9), and is not within the supporting hole. Similarly, the solder ball 111 of Kiumura is not formed within the supporting hole 112e. Instead, the solder ball 111 simply lies outside the supporting hole 112e (Fig 9).

Therefore, in view of the foregoing reasons, even Kimura is combined with APA, the combination still fails to teach or suggest the claimed invention. Accordingly, the withdrawal of the rejection and the allowance of claims 1 and 5 are earnestly requested. Because claims 3, 6-7 and 9 are dependent upon claims 1 and 5 respectively, the same reasons as discussed above also apply to these claims.

Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiumura (US Patent Application 2003/0151139) in view of admitted prior art (APA), and further in view of Kikuchi et al. (USP 5122860, Kikuchi hereinafter).

Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiumura (US Patent Application 2003/0151139) in view of admitted prior art (APA), and further in view **of Murata et al. (USP 6400010).**

With regard to the rejections of claims 2 and 8 by Kiumura in view of APA and further in view of Kikuchi and the rejections of claims 4 and 10 by Kiumura in view of APA and further in view of Murata, Applicant respectfully submits that these claims patently define over the prior art for at least the same reasons as independent claims 1 and 5 discussed above. Reconsideration and withdrawal of the rejection is courteously requested.

Newly Added Claims

Applicants have added claims 11-15, wherein claim 11 is written in independent form combining the features of a plurality of solid conductive columns disposed within the respective columnar through holes and a plurality of dielectric walls disposed between the sidewall of the conductive columns and the inner surface of the corresponding columnar through holes so as to further limit the claimed subject matter of the present invention. Therefore, it is believed claims 11-15 are patentable for the above reasons.

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CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 1-15, are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Sept. 27, 2004

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